Apple 1 32K and 20K Memory Upgrade

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This document describes memory upgrades for an Apple 1 or Clone Board. The first design was used on my board in about 1980 and represents the type of modification that was common for hobbyists of that era. Many Apple 1 boards were modified because they were intended for hardware and software tinkerers.

32K Board Mod

This design supports the installation of 16 16K DRAMS in the memory positions on the Apple 1 board. The memory chips must be the 3 power supply variety, not the single 5 volt parts. Figure 1 shows the cuts that were made on the board for this modification.

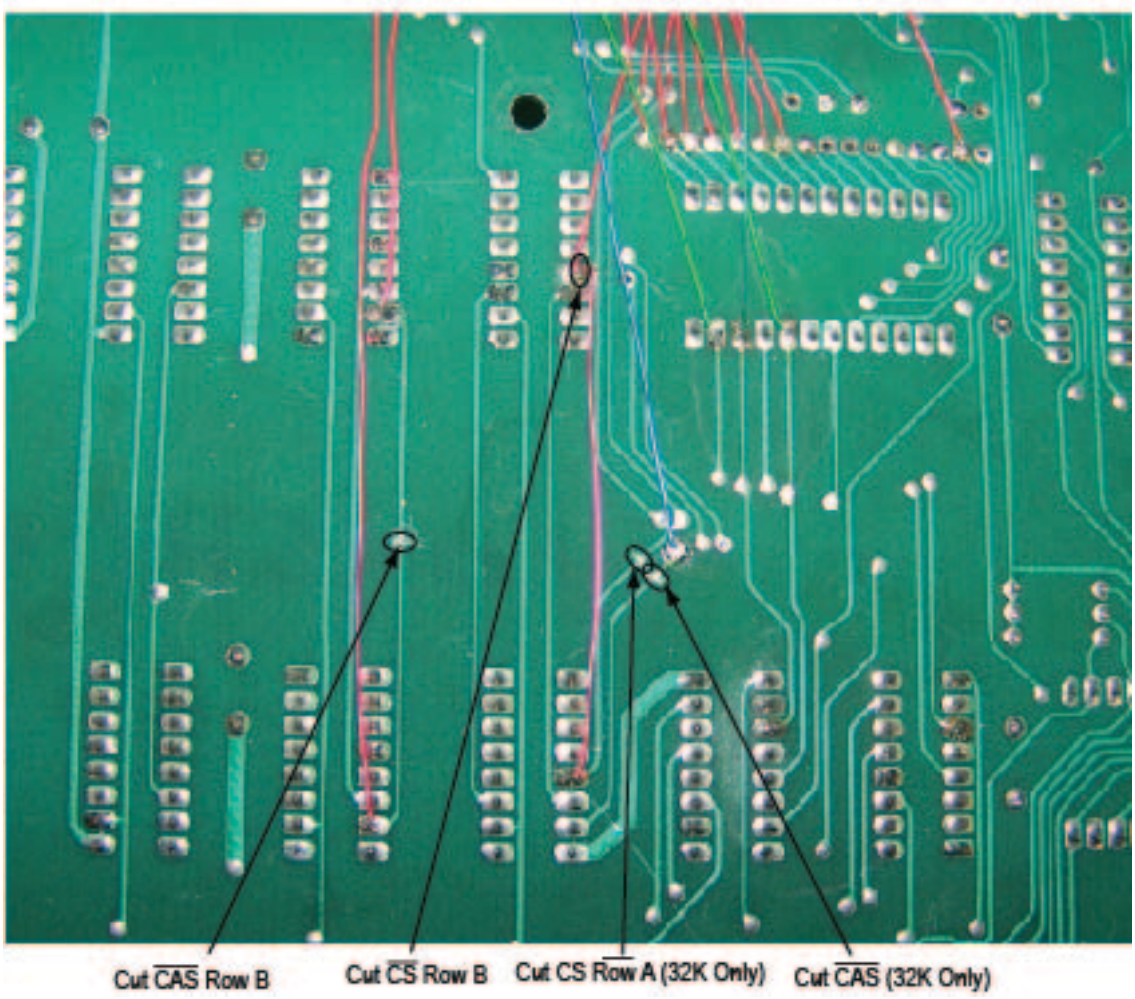

Figure 1

If you don't have the nerve to make cuts on a $300,000 collectable board the same result can be accomplished by lifting pins 13 and 15 on all 16 DRAMS then connect all pin 13's together and then connect all pin 15's on each row together. This is not very esthetically pleasing when looking at the top of the Board but no cuts are needed. Figure 2 illustrates the Schematic of the modification.

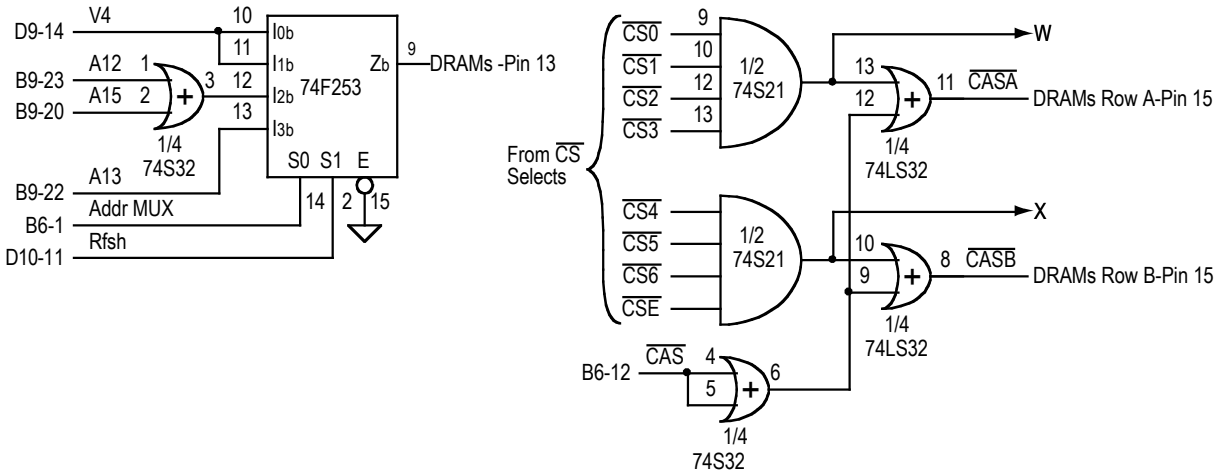

Figure 2

Three IC's need to be added, a 74S32 or 74F32, 74LS21, and a 74S253 or 74F253. The 253 multiplexer needs to be a fast part to assure Address set-up time to /CAS. The extra S32 gate is used to add delay to the /CAS signal for added margin but is not required, the S32 is needed to provide good drive to the /CAS lines. This design maps the DRAM memory from $0000 to $6FFF with no breaks and $E000 to $EFFF.

This design provides the maximum flexibility for address remapping for peripherals using the /CS connections. The bottom view of the board is shown in Figure 3, no sign of the modification is seen on the top of the board except for the added parts in the BB space. The interconnection style using wire wrap wire stretched tight is very similar to Woz's assembly style.

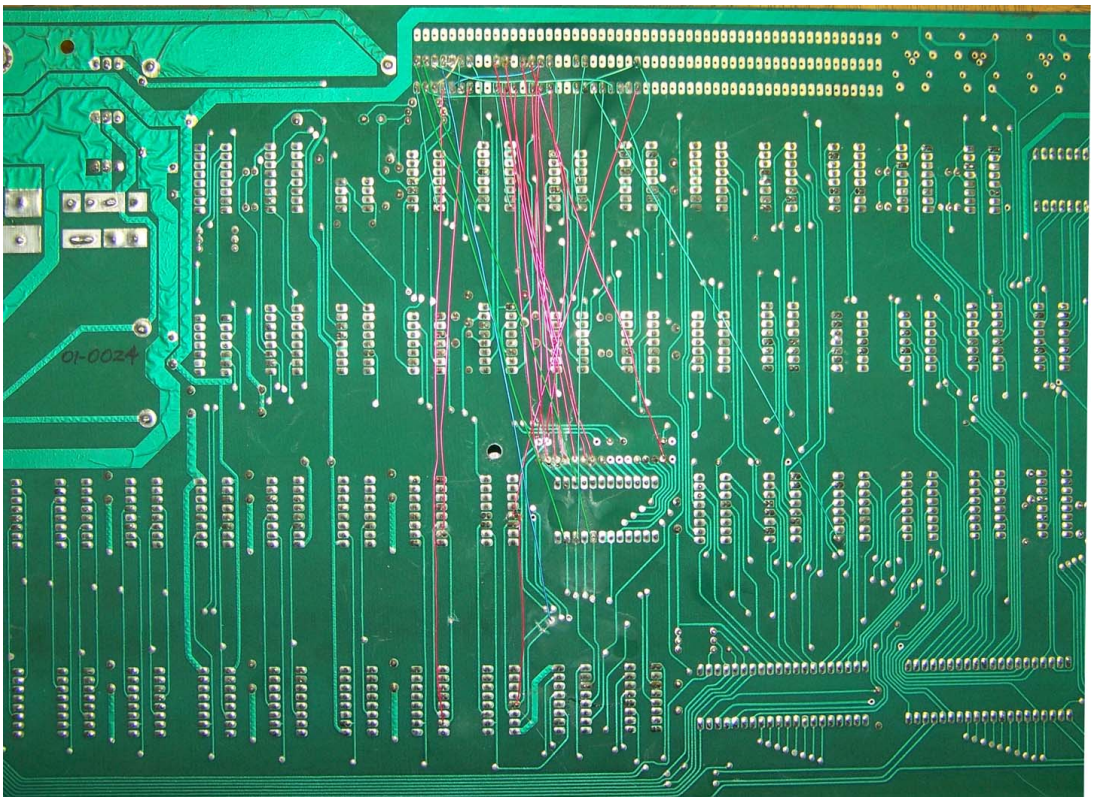

Figure 3

A simpler version is shown in Figure 4. This solution only requires 2 added parts a 74S or 74F251 and 74S or 74F32 and uses spare parts from the Apple 1 Board.

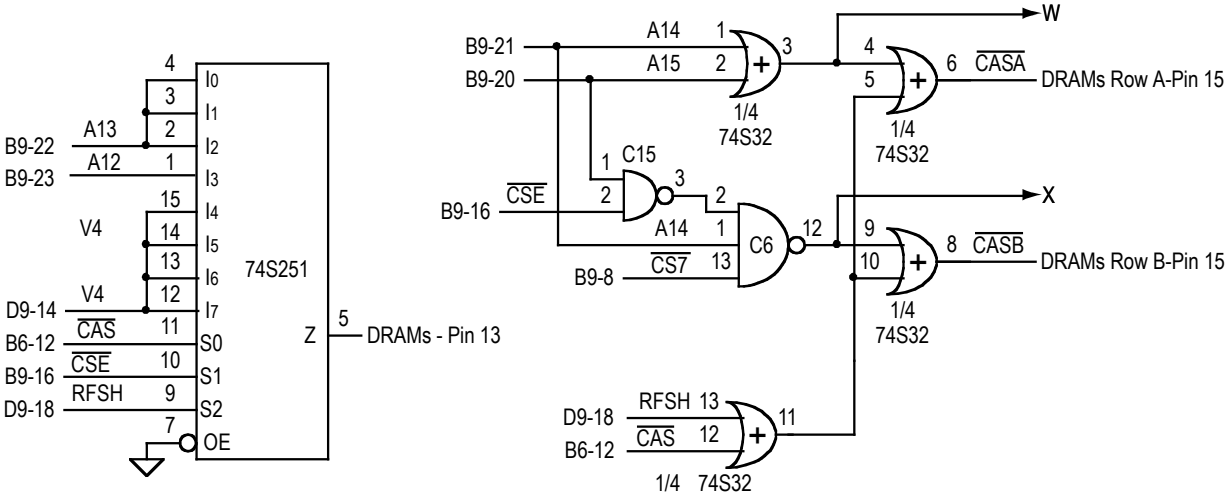

Figure 4

This version uses the /CAS to multiplex the address. This works well for the MK 4116 because it has a negative Address Setup time to /CAS. This was a change

from the MK4096 which had a zero set-up time. That change was made based on input from the DRAM users. Also the /CAS goes through two gate delays whereas the Address goes through one gate delay. The RFSH is taken from the Enable on the enable on the 74154 which is the complement of RF on the connector because VMA is wired high.

20K Board Mod

A 20K version of the circuit of Figure 4 requires only the 74F or 74S253 and 74F or 74S32. Only the DRAMs in Row B are 16K in this case. Figure 5 shows the schematic for this implementation.

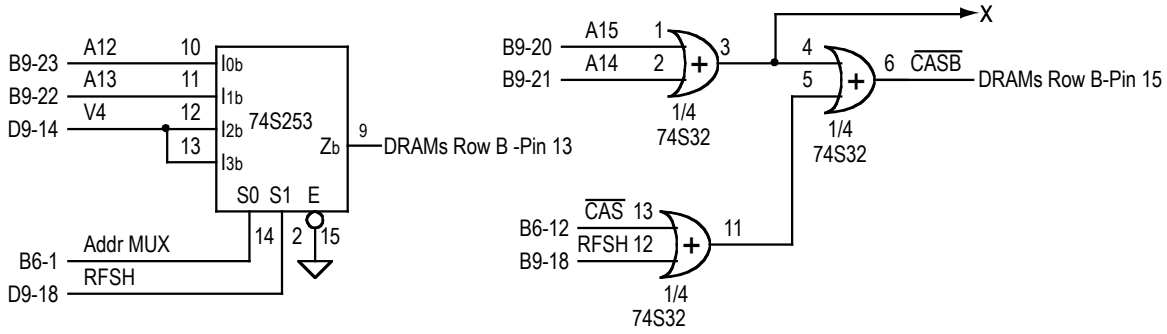

Figure 5

This 16K of added memory is mapped from $0000 to $3FFF with no breaks. The 4K bank of DRAMS in Row A would normally be mapped to $E000 to $EFFF.